

Please add new claim 10 as follows:

c3 10. (New) The input circuit of claim 3, wherein said edge of the clock signal on which the data signal is intended to be latched is provided to said comparator without being subject to a delay.

REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended claim 2 into independent format. In addition, claim 9 has been amended as suggested by the Examiner in order to overcome the pending rejection thereof under 35 U.S.C. § 112, second paragraph. Applicants would like to thank the Examiner for his assistance in suggesting acceptable claim language. In addition, Applicants would like to thank the Examiner for the indication that claims 4 and 8 are allowable, and that claims 2 and 9 would be allowable if amended in the manner set forth above. Finally, new claim 10 has been added to recite an additional aspect of the present invention not previously claimed. No new matter has been added.

Applicants respectfully traverse the rejection of claims 3 and 5 for the reasons set forth below.

II. The Rejection Of Claim 9 Under 35 U.S.C. § 112

Claim 9 was rejected under 35 U.S.C. § 112, second paragraph. In response,

Applicants have amended claim 9 in accordance with the Examiner's suggestion for overcoming the rejection. As such, it is respectfully submitted that the rejection has been overcome.

III. The Rejection Of The Claims In View of Suzuki

Claims 3 and 5 were rejected under 35 U.S.C. § 102 as being anticipated by USP No. 5,952,857 to Suzuki. Applicants respectfully traverse this rejection for the following reasons.

As recited by claim 3, the delay means comprises ***a comparator for comparing the edge of the clock signal, on which the data signal is intended to be latched***, to at least one of the leading and trailing edges of the data signal, and a delay circuit for defining the delay time based on a result of this comparison. In accordance with the foregoing element, the comparator receives as one input an undelayed clock signal (i.e., the edge of the clock signal on which the data signal is intended to be latched), while the other input to the comparator receives an undelayed data signal. This is shown clearly in Fig. 1 of the specification, which illustrates that the CLK signal is fed directly into the comparator 5.

In contrast, referring to Fig. 1 of Suzuki, it is shown that the CLK signal is coupled to the phase-comparison circuit 20 by means of a delay circuit 22. Thus, at a minimum, the phase-comparator circuit 20 of Suzuki does not receive the edge of the clock signal on which the data signal is intended to be latched, and therefore fails to

satisfy the foregoing limitation. Indeed, it is noted that the operation of Suzuki is wholly different from that of the present invention. For example, in Suzuki, when each of the transition timings of the input signals are different, the input signals are delayed such that the transition timings are in synchronism with the latest transition timing among the transition timings, and the clock signal is also delayed in accordance with this delay amount. In the present invention, there is no delay of the input data. Moreover, as noted above, the clock signal of the present invention is not delayed prior to being coupled to the comparator.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), for the foregoing reasons, it is clear that Suzuki does not anticipate claim 3, or any claim dependent thereon.

IV. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an

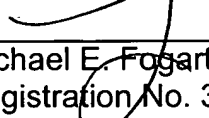
Serial No.: 09/299,659

Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 6/30/03

By: 
Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W. , Suite 1200
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087

WDC99 778047-1.043889.0861

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 2 and 9 have been amended, and new claim 10 has been added as follows:

2. (Twice Amended) [The] An input circuit [of Claim 3] comprising:
delay means for defining a delay time for at least one logical state of a data
signal and thereby delaying a clock signal for the delay time defined; and
a holding circuit for holding the data signal responsive to the delayed clock
signal;

wherein the delay means comprises:

a comparator for comparing an edge of the clock signal, on which the data
signal is intended to be latched, to at least one of leading and trailing edges of the data
signal; and

a delay circuit for defining the delay time based on a result of comparison
performed by the comparator, and

wherein the delay means defines the delay time such that an edge of the clock signal, on which the data signal is intended to be latched and which is included within a transition interval of the data signal, is delayed to a point in time after the transition interval of the data signal is over.

9. (Amended) The input circuit of claim 4, wherein the first delay circuit defines

the delay time based on the result of comparison performed by the comparator,
between one of the leading edges of the data signal and the edge of the clock signal,
and a setup time for correctly latching the data signal, and the second delay circuit
defines the delay time based on the result of comparison performed by the comparator,
between one of the trailing edges of the data signal and the edge of the clock signal,
and the setup time for correctly latching the data signal.

Please add new claim 10 as follows:

10. (New) The input circuit of claim 3, wherein said edge of the clock signal on which the data signal is intended to be latched is provided to said comparator without being subject to a delay.